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Implementing Complex Clock Designs in Field Programmable Devices

Abstract

An aspect of the present invention simplifies the implementation of complex clock designs in field programmable devices (FPD). To implement a circuit logic containing base sequential elements (e.g., D flip-flops) with corresponding circuit clocks, a number of modified sequential elements equaling the number of base sequential elements may be employed. Each modified sequential element (contained in FPD) receives a global clock, corresponding circuit clock and a data value. A base sequential element (contained in modified sequential element) transitions to a next state only after occurrence of a transition on a corresponding circuit clock and the transition to said next state may be timed according to the global clock. By timing the transitions according to the global clock, several undesired results may be avoided.